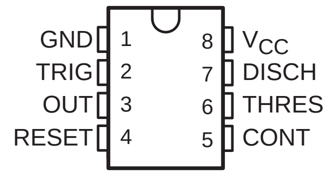
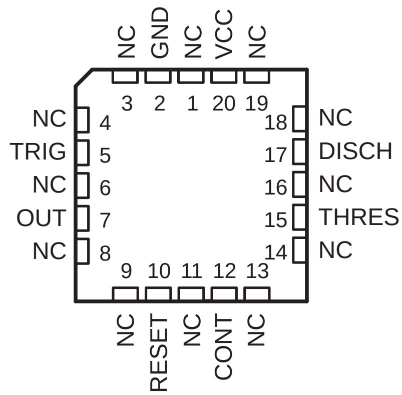
- **Timing From Microseconds to Hours**
- **Astable or Monostable Operation**
- **Adjustable Duty Cycle**
- **TTL-Compatible Output Can Sink or Source Up To 200 mA**

**NE555 . . . D, P, PS, OR PW PACKAGE**
**SA555 . . . D OR P PACKAGE**
**SE555 . . . D, JG, OR P PACKAGE**
**(TOP VIEW)**




**SE555 . . . FK PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## description/ordering information

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of $V_{CC}$. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

## description/ordering information (continued)

### ORDERING INFORMATION

| $T_A$ | $V_{THRES}$ MAX $V_{CC}$ = 15 V | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|---|
| 0°C to 70°C | 11.2 V | PDIP (P) | Tube of 50 | NE555P | NE555P |
| | | SOIC (D) | Tube of 75 | NE555D | NE555 |
| | | | Reel of 2500 | NE555DR | |
| | | SOP (PS) | Reel of 2000 | NE555PSR | N555 |
| | | TSSOP (PW) | Tube of 150 | NE555PW | N555 |
| | | | Reel of 2000 | NE555PWR | |
| −40°C to 85°C | 11.2 V | PDIP (P) | Tube of 50 | SA555P | SA555P |
| | | SOIC (D) | Tube of 75 | SA555D | SA555 |
| | | | Reel of 2000 | SA555DR | |
| −55°C to 125°C | 10.6 V | PDIP (P) | Tube of 50 | SE555P | SE555P |
| | | SOIC (D) | Tube of 75 | SE555D | SE555D |
| | | | Reel of 2500 | SE555DR | |
| | | CDIP (JG) | Tube of 50 | SE555JG | SE555JG |
| | | LCCC (FK) | Tube of55 | SE555FK | SE555FK |

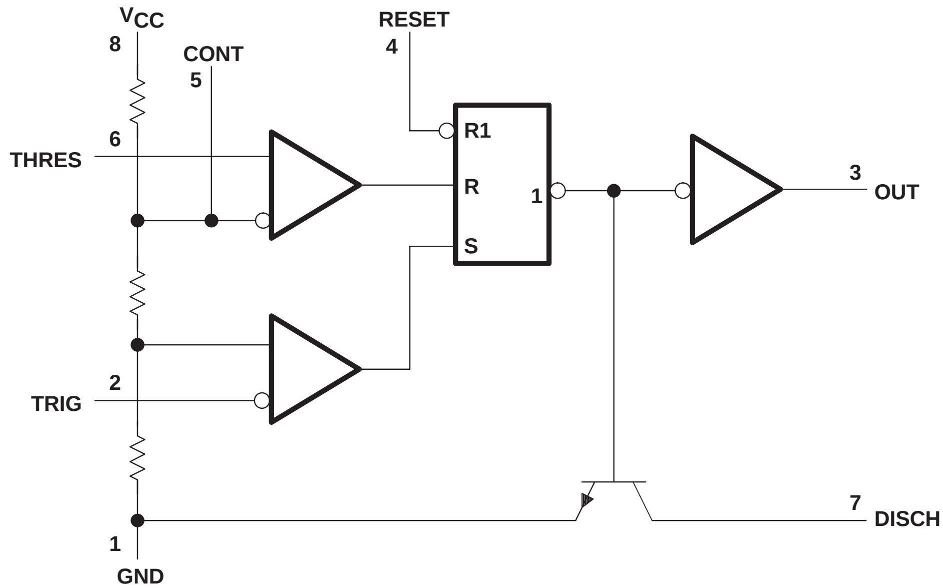
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**

| RESET | TRIGGER VOLTAGE‡ | THRESHOLD VOLTAGE‡ | OUTPUT | DISCHARGE SWITCH |
|---|---|---|---|---|
| Low | Irrelevant | Irrelevant | Low | On |
| High | <1/3 $V_{DD}$ | Irrelevant | High | Off |
| High | >1/3 $V_{DD}$ | >2/3 $V_{DD}$ | Low | On |
| High | >1/3 $V_{DD}$ | <2/3 $V_{DD}$ | As previously established | |

‡ Voltage levels shown are nominal.

## functional block diagram




Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: RESET can override TRIG, which can override THRES.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) . . . 18 V
Input voltage (CONT, RESET, THRES, and TRIG) . . . $V_{CC}$
Output current . . . ±225 mA
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): D package . . . 97°C/W
P package . . . 85°C/W
PS package . . . 95°C/W
PW package . . . 149°C/W
Package thermal impedance, $\theta_{JC}$ (see Notes 4 and 5): FK package . . . 5.61°C/W
JG package . . . 14.5°C/W
Operating virtual junction temperature, $T_J$ . . . 150°C
Case temperature for 60 seconds: FK package . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . 300°C
Storage temperature range, $T_{stg}$ . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Maximum power dissipation is a function of $T_J$(max), $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. Maximum power dissipation is a function of $T_J$(max), $\theta_{JC}$, and $T_C$. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) - T_C)/\theta_{JC}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with MIL-STD-883.

## recommended operating conditions

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | SA555, NE555 | 4.5 | 16 | V |
| | | SE555 | 4.5 | 18 | |
| $V_I$ | Input voltage (CONT, RESET, THRES, and TRIG) | | | $V_{CC}$ | V |
| $I_O$ | Output current | | | ±200 | mA |
| $T_A$ | Operating free-air temperature | NE555 | 0 | 70 | °C |
| | | SA555 | −40 | 85 | |
| | | SE555 | −55 | 125 | |

## electrical characteristics, $V_{CC}$ = 5 V to 15 V, $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SE555 | | | NE555 SA555 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| THRES voltage level | $V_{CC}$ = 15 V | | 9.4 | 10 | 10.6 | 8.8 | 10 | 11.2 | V |
| | $V_{CC}$ = 5 V | | 2.7 | 3.3 | 4 | 2.4 | 3.3 | 4.2 | |
| THRES current (see Note 6) | | | | 30 | 250 | | 30 | 250 | nA |
| TRIG voltage level | $V_{CC}$ = 15 V | | 4.8 | 5 | 5.2 | 4.5 | 5 | 5.6 | V |
| | | $T_A$ = −55°C to 125°C | 3 | | 6 | | | | |
| | $V_{CC}$ = 5 V | | 1.45 | 1.67 | 1.9 | 1.1 | 1.67 | 2.2 | |
| | | $T_A$ = −55°C to 125°C | | | 1.9 | | | | |
| TRIG current | TRIG at 0 V | | | 0.5 | 0.9 | | 0.5 | 2 | μA |
| RESET voltage level | | | 0.3 | 0.7 | 1 | 0.3 | 0.7 | 1 | V |
| | $T_A$ = −55°C to 125°C | | | | 1.1 | | | | |
| RESET current | RESET at $V_{CC}$ | | | 0.1 | 0.4 | | 0.1 | 0.4 | mA |
| | RESET at 0 V | | | −0.4 | −1 | | −0.4 | −1.5 | |
| DISCH switch off-state current | | | | 20 | 100 | | 20 | 100 | nA |
| CONT voltage (open circuit) | $V_{CC}$ = 15 V | | 9.6 | 10 | 10.4 | 9 | 10 | 11 | V |
| | | $T_A$ = −55°C to 125°C | 9.6 | | 10.4 | | | | |
| | $V_{CC}$ = 5 V | | 2.9 | 3.3 | 3.8 | 2.6 | 3.3 | 4 | |
| | | $T_A$ = −55°C to 125°C | 2.9 | | 3.8 | | | | |
| Low-level output voltage | $V_{CC}$ = 15 V, $I_{OL}$ = 10 mA | | | 0.1 | 0.15 | | 0.1 | 0.25 | V |
| | | $T_A$ = −55°C to 125°C | | | 0.2 | | | | |
| | $V_{CC}$ = 15 V, $I_{OL}$ = 50 mA | | | 0.4 | 0.5 | | 0.4 | 0.75 | |
| | | $T_A$ = −55°C to 125°C | | | 1 | | | | |
| | $V_{CC}$ = 15 V, $I_{OL}$ = 100 mA | | | 2 | 2.2 | | 2 | 2.5 | |
| | | $T_A$ = −55°C to 125°C | | | 2.7 | | | | |
| | $V_{CC}$ = 15 V, | $I_{OL}$ = 200 mA | | 2.5 | | | 2.5 | | |
| | $V_{CC}$ = 5 V, $I_{OL}$ = 3.5 mA | $T_A$ = −55°C to 125°C | | | 0.35 | | | | |
| | $V_{CC}$ = 5 V, $I_{OL}$ = 5 mA | | | 0.1 | 0.2 | | 0.1 | 0.35 | |
| | | $T_A$ = −55°C to 125°C | | | 0.8 | | | | |
| | $V_{CC}$ = 5 V, | $I_{OL}$ = 8 mA | | 0.15 | 0.25 | | 0.15 | 0.4 | |
| High-level output voltage | $V_{CC}$ = 15 V, $I_{OH}$ = −100 mA | | 13 | 13.3 | | 12.75 | 13.3 | | V |
| | | $T_A$ = −55°C to 125°C | 12 | | | | | | |
| | $V_{CC}$ = 15 V, | $I_{OH}$ = −200 mA | | 12.5 | | | 12.5 | | |
| | $V_{CC}$ = 5 V, $I_{OH}$ = −100 mA | | 3 | 3.3 | | 2.75 | 3.3 | | |
| | | $T_A$ = −55°C to 125°C | 2 | | | | | | |
| Supply current | Output low, No load | $V_{CC}$ = 15 V | | 10 | 12 | | 10 | 15 | mA |
| | | $V_{CC}$ = 5 V | | 3 | 5 | | 3 | 6 | |
| | Output high, No load | $V_{CC}$ = 15 V | | 9 | 10 | | 9 | 13 | |
| | | $V_{CC}$ = 5 V | | 2 | 4 | | 2 | 5 | |

NOTE 6: This parameter influences the maximum value of the timing resistors $R_A$ and $R_B$ in the circuit of Figure 12. For example, when $V_{CC}$ = 5 V, the maximum value is R = $R_A$ + $R_B$ ≈ 3.4 MΩ, and for $V_{CC}$ = 15 V, the maximum value is 10 MΩ.

## operating characteristics, $V_{CC}$ = 5 V and 15 V

| PARAMETER | | TEST CONDITIONS† | SE555 | | | NE555 SA555 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Initial error of timing interval‡ | Each timer, monostable§ | $T_A$ = 25°C | | 0.5 | 1.5* | | 1 | 3 | % |
| | Each timer, astable¶ | | | 1.5 | | | 2.25 | | |
| Temperature coefficient of timing interval | Each timer, monostable§ | $T_A$ = MIN to MAX | | 30 | 100* | | 50 | | ppm/°C |
| | Each timer, astable¶ | | | 90 | | | 150 | | |
| Supply-voltage sensitivity of timing interval | Each timer, monostable§ | $T_A$ = 25°C | | 0.05 | 0.2* | | 0.1 | 0.5 | %/V |
| | Each timer, astable¶ | | | 0.15 | | | 0.3 | | |
| Output-pulse rise time | | $C_L$ = 15 pF, $T_A$ = 25°C | | 100 | 200* | | 100 | 300 | ns |
| Output-pulse fall time | | $C_L$ = 15 pF, $T_A$ = 25°C | | 100 | 200* | | 100 | 300 | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
§ Values specified are for a device in a monostable circuit similar to Figure 9, with the following component values: $R_A$ = 2 kΩ to 100 kΩ, C = 0.1 µF.
¶ Values specified are for a device in an astable circuit similar to Figure 12, with the following component values: $R_A$ = 1 kΩ to 100 kΩ, C = 0.1 µF.

## TYPICAL CHARACTERISTICS†

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

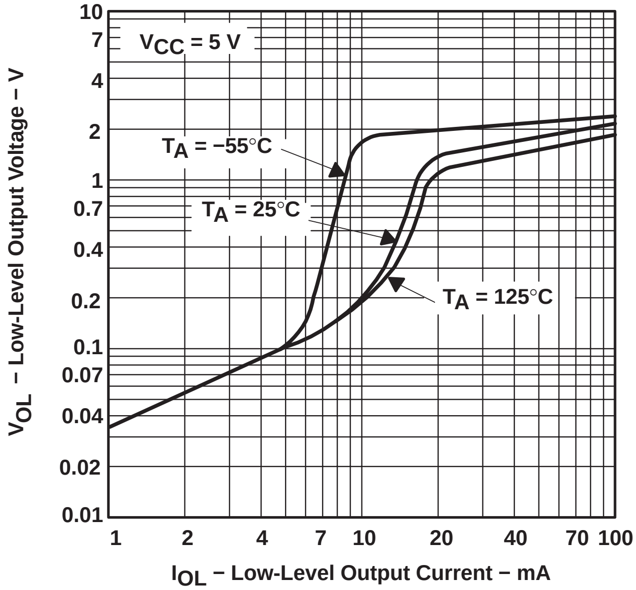



**Figure 1**

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

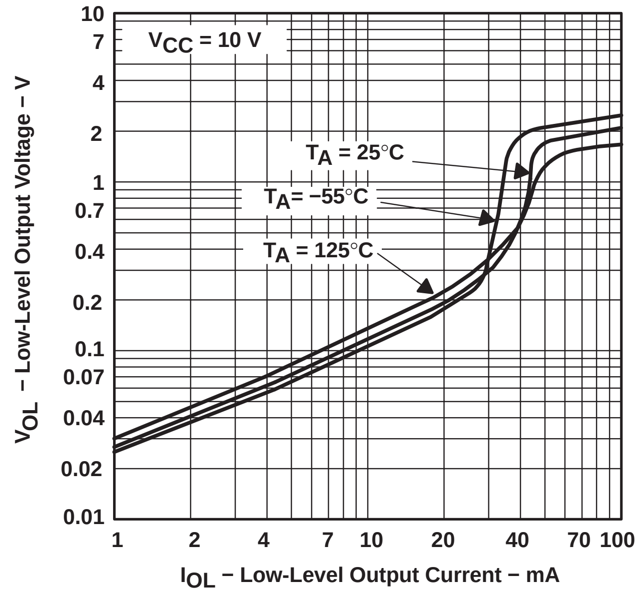



**Figure 2**

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

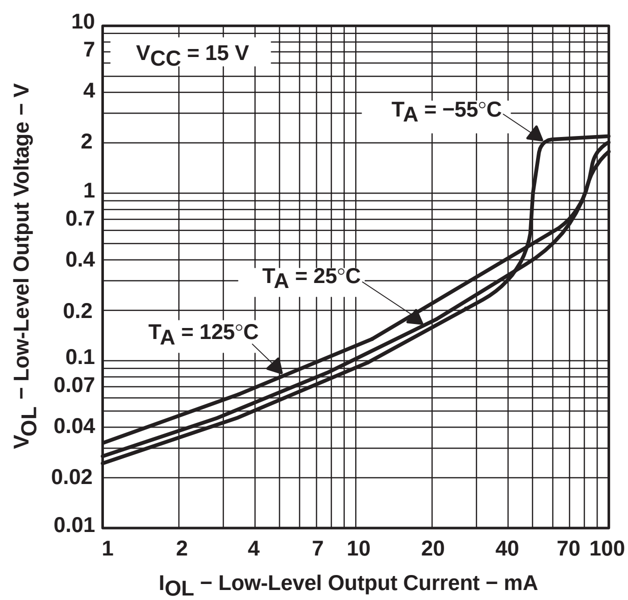



**Figure 3**

**DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT
vs
HIGH-LEVEL OUTPUT CURRENT**

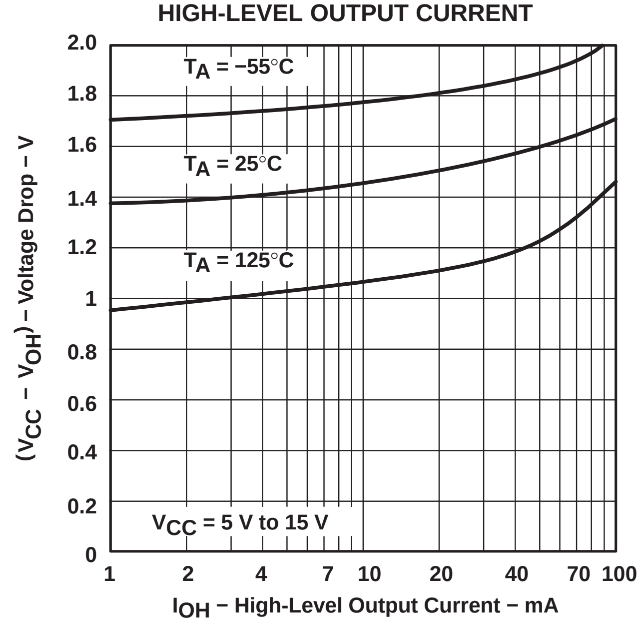



**Figure 4**

†Data for temperatures below 0°C and above 70°C are applicable for SE555 circuits only.

## TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

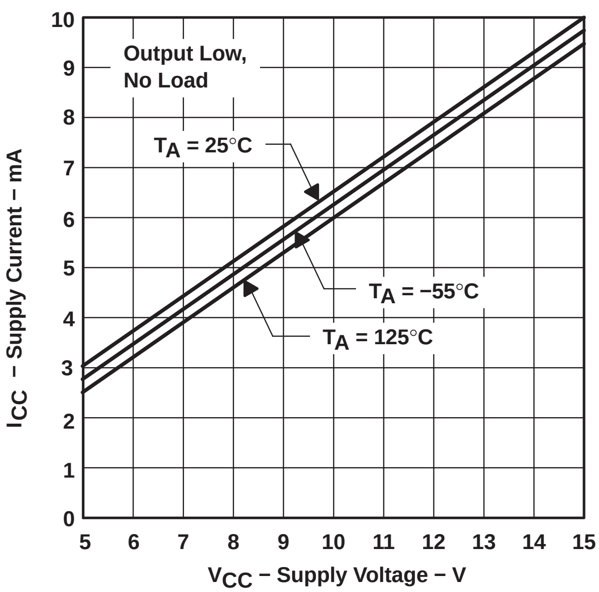



Figure 5

NORMALIZED OUTPUT PULSE DURATION
(MONOSTABLE OPERATION)
vs
SUPPLY VOLTAGE

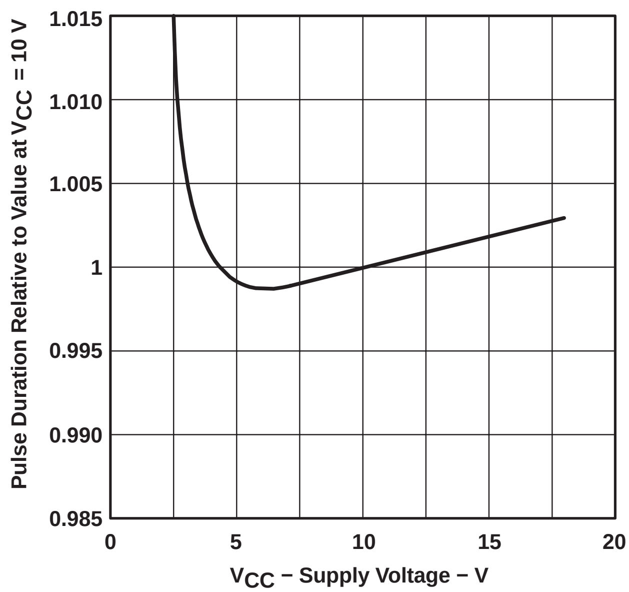



Figure 6

NORMALIZED OUTPUT PULSE DURATION
(MONOSTABLE OPERATION)
vs
FREE-AIR TEMPERATURE

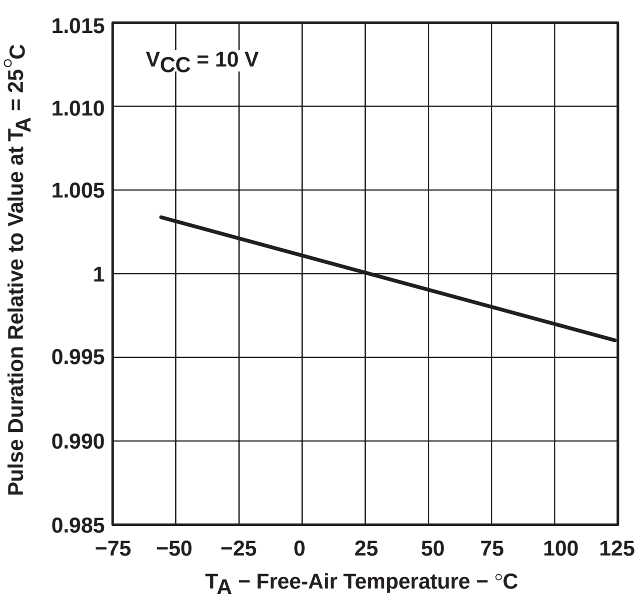



Figure 7

PROPAGATION DELAY TIME
vs
LOWEST VOLTAGE LEVEL
OF TRIGGER PULSE

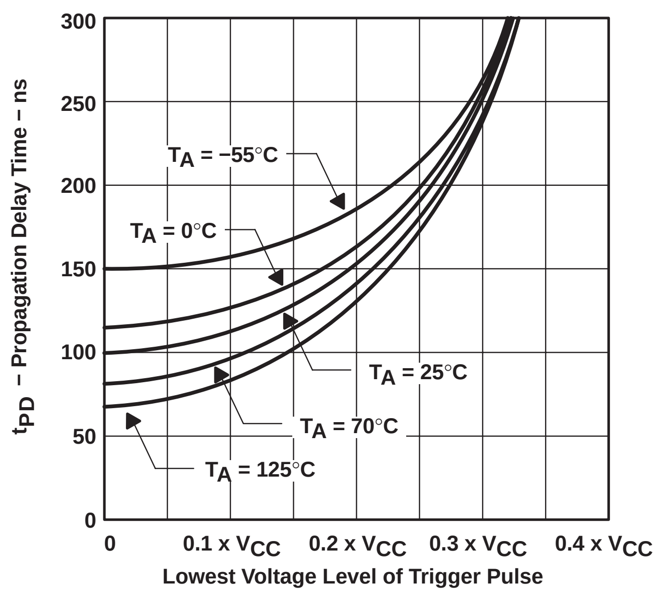


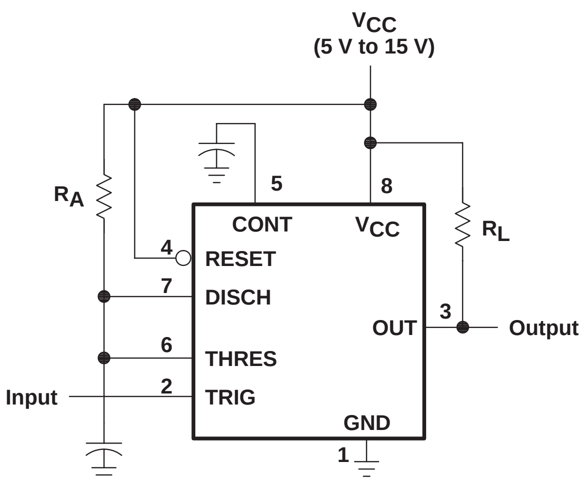

Figure 8

†Data for temperatures below 0°C and above 70°C are applicable for SE555 series circuits only.

## APPLICATION INFORMATION

### monostable operation

For monostable operation, any of these timers can be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C then is charged through $R_A$ until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop ($\overline{Q}$ goes high), drives the output low, and discharges C through Q1.




Pin numbers shown are for the D, JG, P, PS, and PW packages.

**Figure 9. Circuit for Monostable Operation**

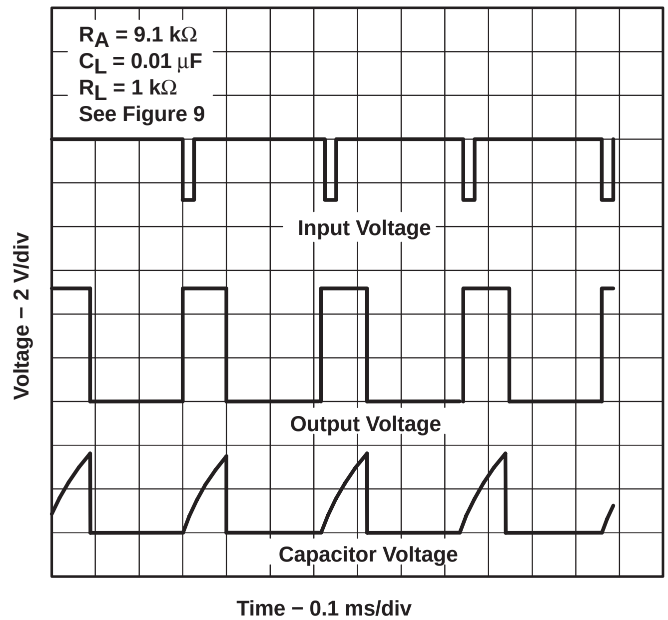



**Figure 10. Typical Monostable Waveforms**

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_AC$. Figure 11 is a plot of the time constant for various values of $R_A$ and C. The threshold levels and charge rates both are directly proportional to the supply voltage, $V_{CC}$. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to $V_{CC}$.

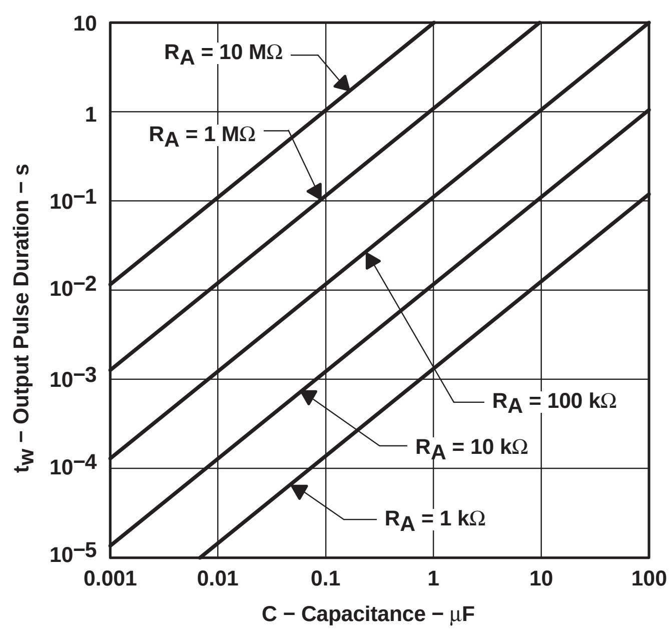


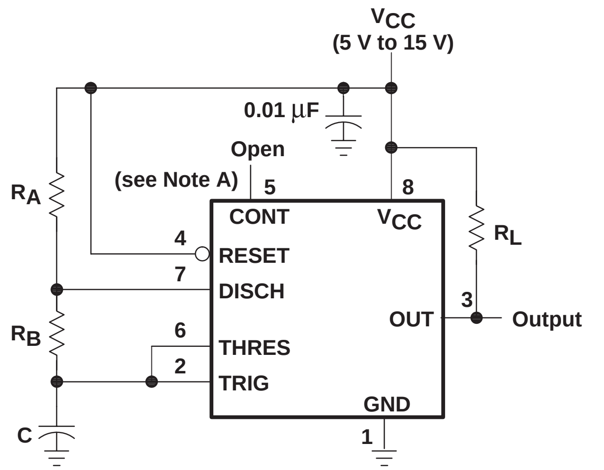

**Figure 11. Output Pulse Duration vs Capacitance**

## APPLICATION INFORMATION

### astable operation

As shown in Figure 12, adding a second resistor, $R_B$, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C charges through $R_A$ and $R_B$ and then discharges through $R_B$ only. Therefore, the duty cycle is controlled by the values of $R_A$ and $R_B$.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \times V_{CC}$) and the trigger-voltage level ($\approx 0.33 \times V_{CC}$). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.




Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

**Figure 12. Circuit for Astable Operation**

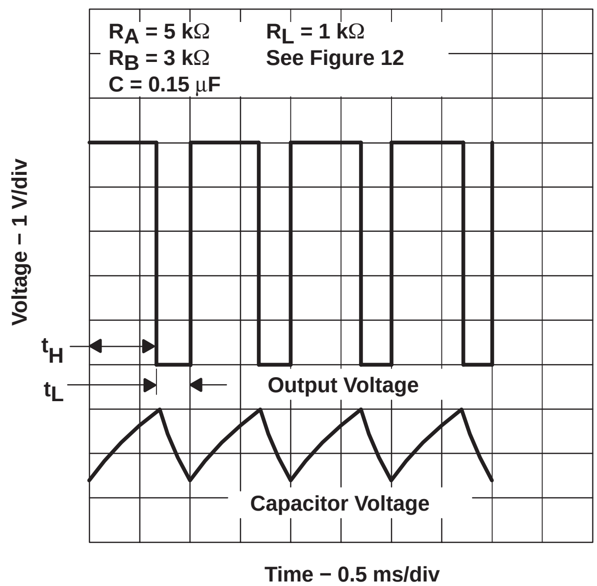



**Figure 13. Typical Astable Waveforms**

## APPLICATION INFORMATION

### astable operation (continued)

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration $t_H$ and low-level duration $t_L$ can be calculated as follows:

$$t_H = 0.693\ (R_A + R_B)\ C$$
$$t_L = 0.693\ (R_B)\ C$$

Other useful relationships are shown below.

$$\text{period} = t_H + t_L = 0.693\ (R_A + 2R_B)\ C$$
$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)\ C}$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B}$$

Output waveform duty cycle

$$= \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B}$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B}$$

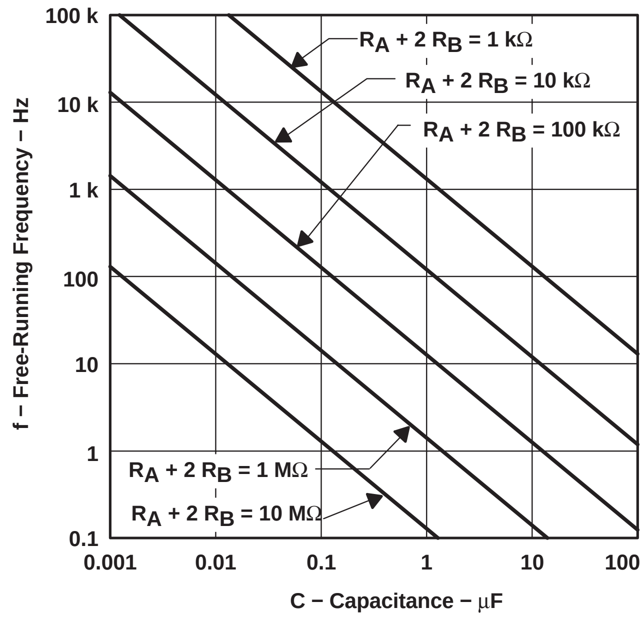
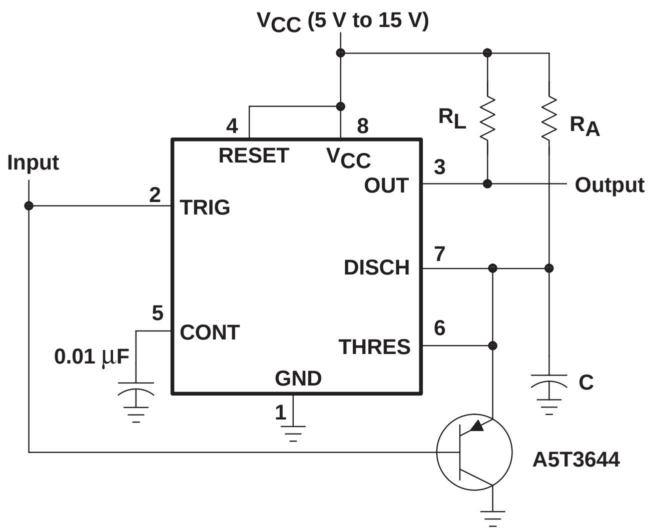



**Figure 14. Free-Running Frequency**

## APPLICATION INFORMATION

### missing-pulse detector

The circuit shown in Figure 15 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is retriggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 16.




Pin numbers shown are shown for the D, JG, P, PS, and PW packages.

**Figure 15. Circuit for Missing-Pulse Detector**

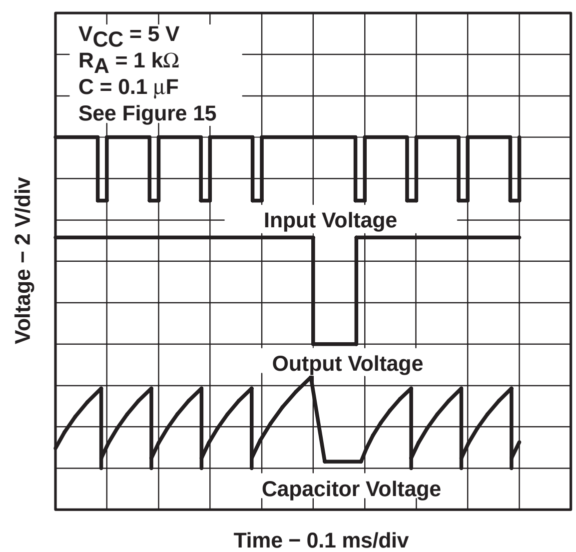



**Figure 16. Completed-Timing Waveforms for Missing-Pulse Detector**

## APPLICATION INFORMATION

### frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 17 shows a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.

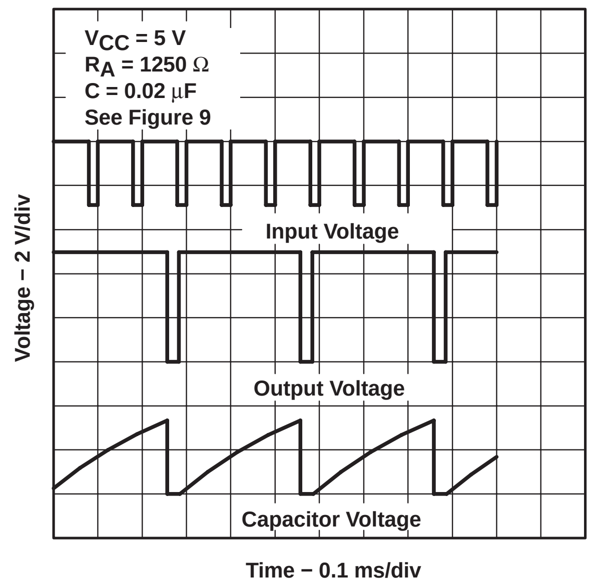
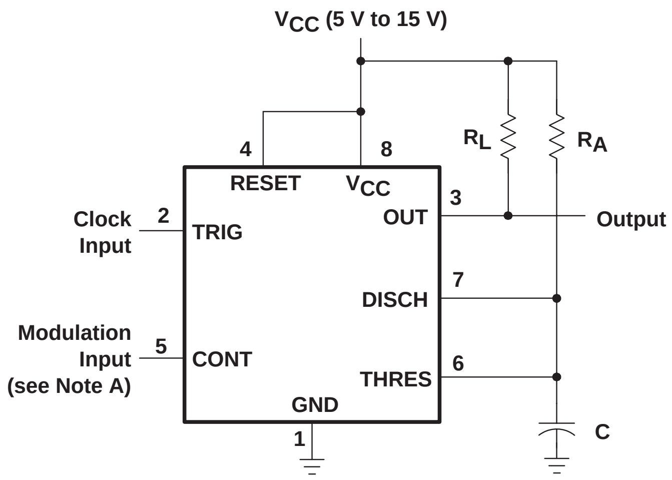



**Figure 17. Divide-by-Three Circuit Waveforms**

### pulse-width modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.

## APPLICATION INFORMATION




Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

**Figure 18. Circuit for Pulse-Width Modulation**

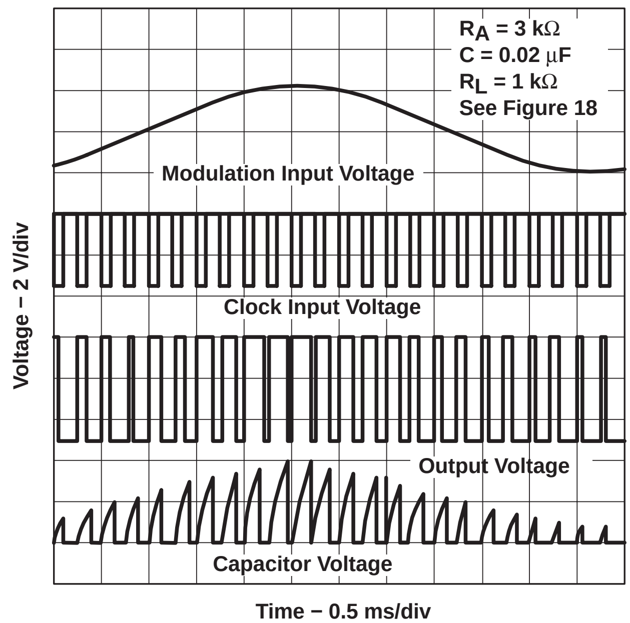
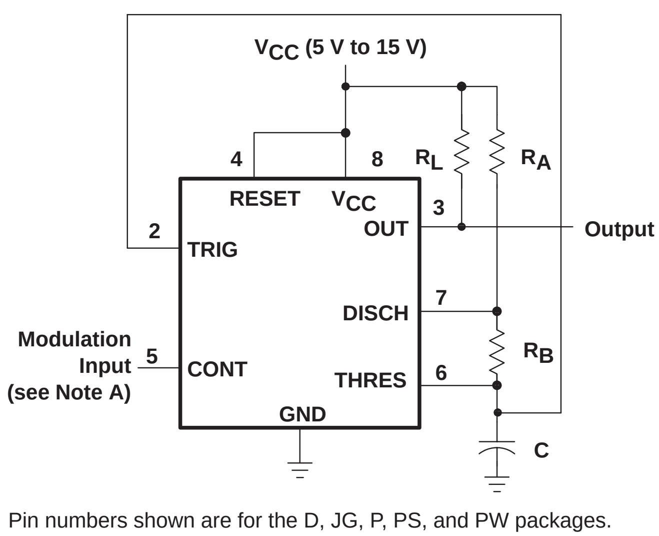



**Figure 19. Pulse-Width-Modulation Waveforms**

### pulse-position modulation

As shown in Figure 20, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 21 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.




Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

**Figure 20. Circuit for Pulse-Position Modulation**

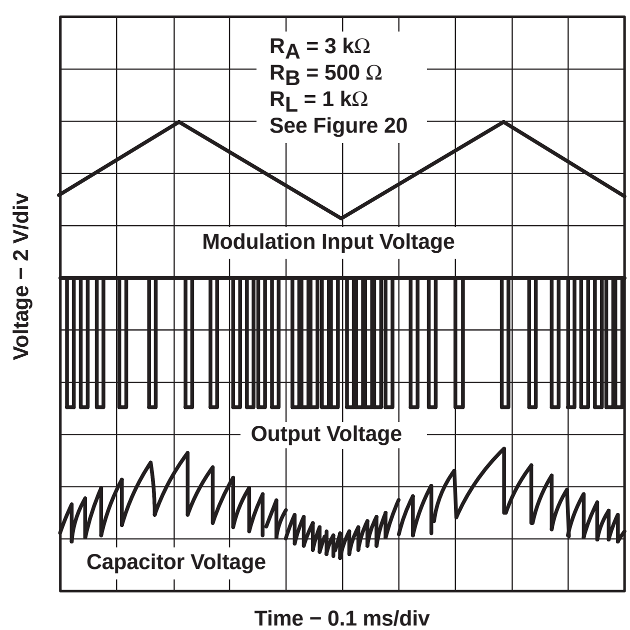
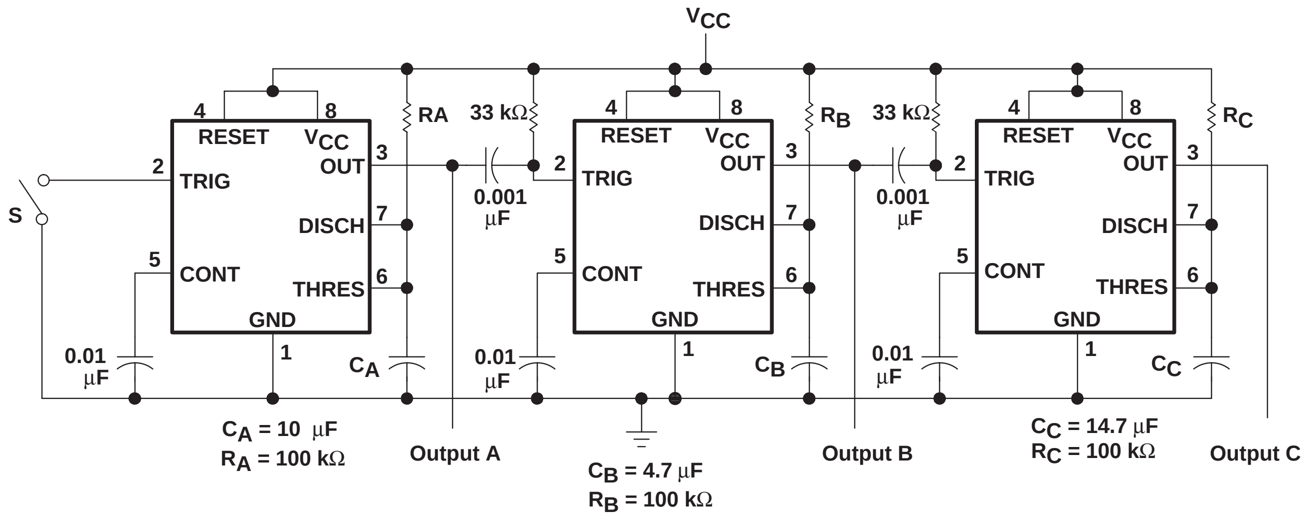



**Figure 21. Pulse-Position-Modulation Waveforms**

## APPLICATION INFORMATION

### sequential timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 shows a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.




Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: S closes momentarily at t = 0.

**Figure 22. Sequential Timer Circuit**

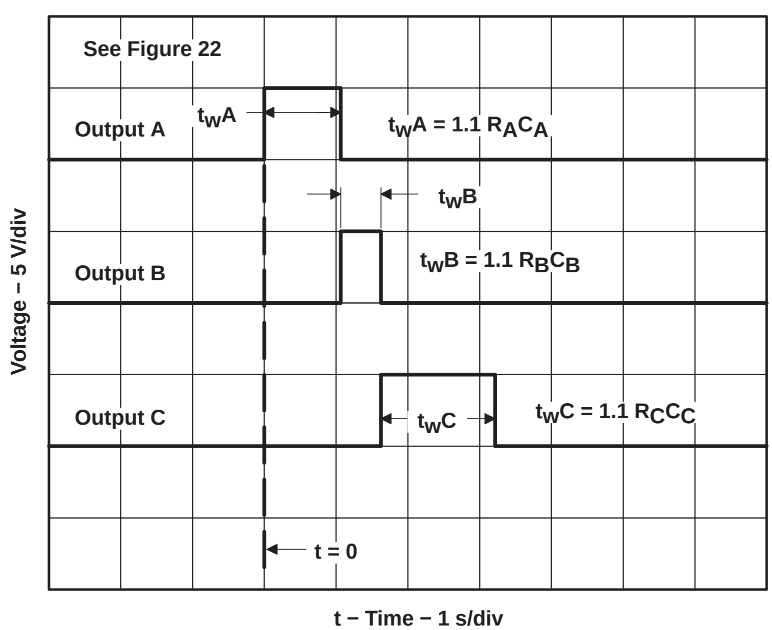



**Figure 23. Sequential Timer Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| JM38510/10901BPA | ACTIVE | CDIP | JG | 8 | 1 | None | A42 SNPB | Level-NC-NC-NC |
| NE555D | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| NE555DR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| NE555P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| NE555PSLE | OBSOLETE | SO | PS | 8 | | None | Call TI | Call TI |
| NE555PSR | ACTIVE | SO | PS | 8 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| NE555PW | ACTIVE | TSSOP | PW | 8 | 150 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| NE555PWR | ACTIVE | TSSOP | PW | 8 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-1-250C-UNLIM |
| NE555Y | OBSOLETE | | | 0 | | None | Call TI | Call TI |
| SA555D | ACTIVE | SOIC | D | 8 | 75 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SA555DR | ACTIVE | SOIC | D | 8 | 2500 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SA555P | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SE555D | ACTIVE | SOIC | D | 8 | 75 | None | CU NIPDAU | Level-1-220C-UNLIM |
| SE555DR | ACTIVE | SOIC | D | 8 | 2500 | None | CU NIPDAU | Level-1-220C-UNLIM |
| SE555FKB | ACTIVE | LCCC | FK | 20 | 1 | None | POST-PLATE | Level-NC-NC-NC |
| SE555JG | ACTIVE | CDIP | JG | 8 | 1 | None | A42 SNPB | Level-NC-NC-NC |
| SE555JGB | ACTIVE | CDIP | JG | 8 | 1 | None | A42 SNPB | Level-NC-NC-NC |
| SE555N | OBSOLETE | PDIP | N | 8 | | None | Call TI | Call TI |
| SE555P | ACTIVE | PDIP | P | 8 | 50 | None | Call TI | Level-NC-NC-NC |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

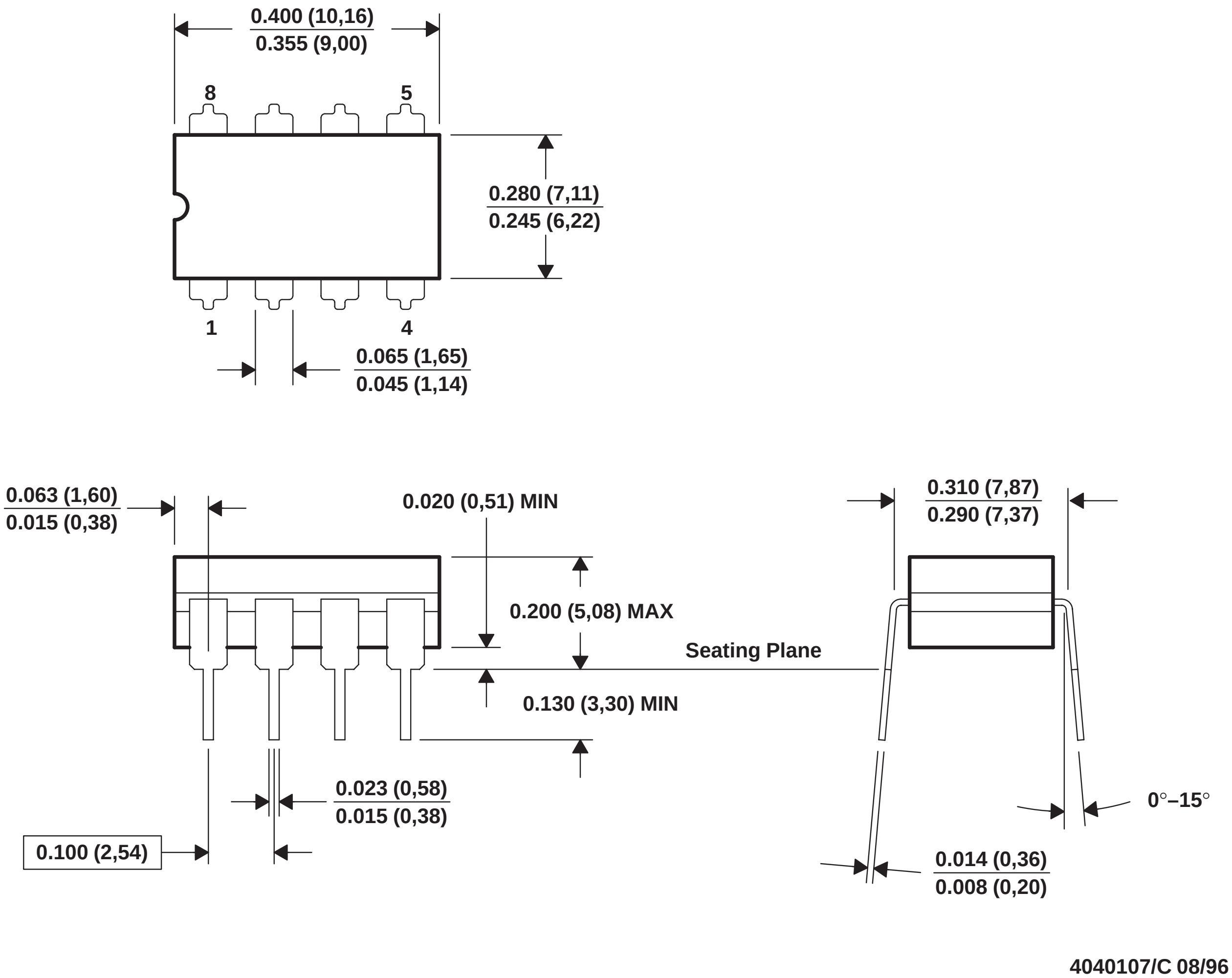
[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**None:** Not yet available Lead (Pb-Free).
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

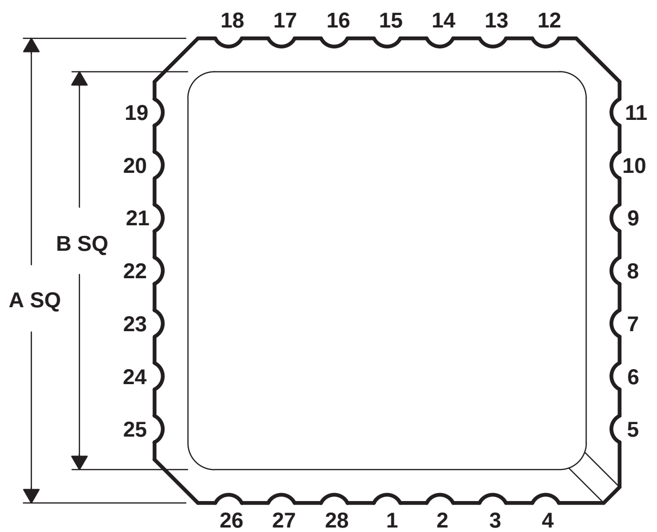
**JG (R-GDIP-T8)** **CERAMIC DUAL-IN-LINE**



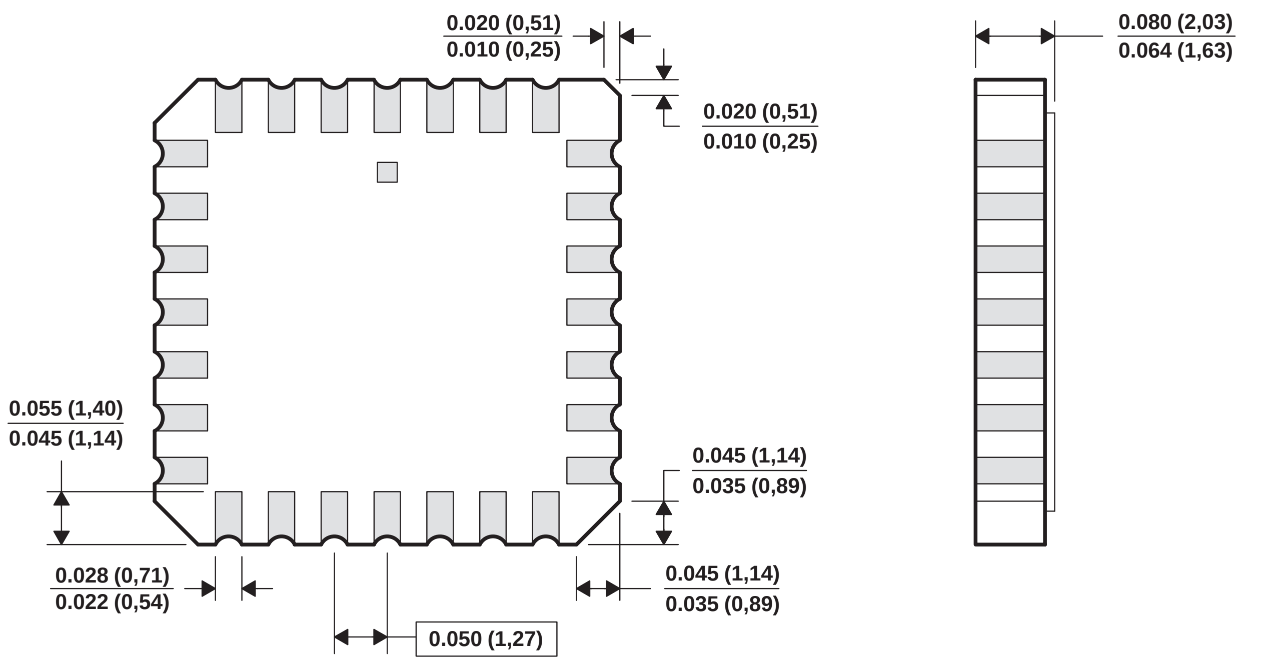

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

**FK (S-CQCC-N**)** **LEADLESS CERAMIC CHIP CARRIER**

**28 TERMINAL SHOWN**



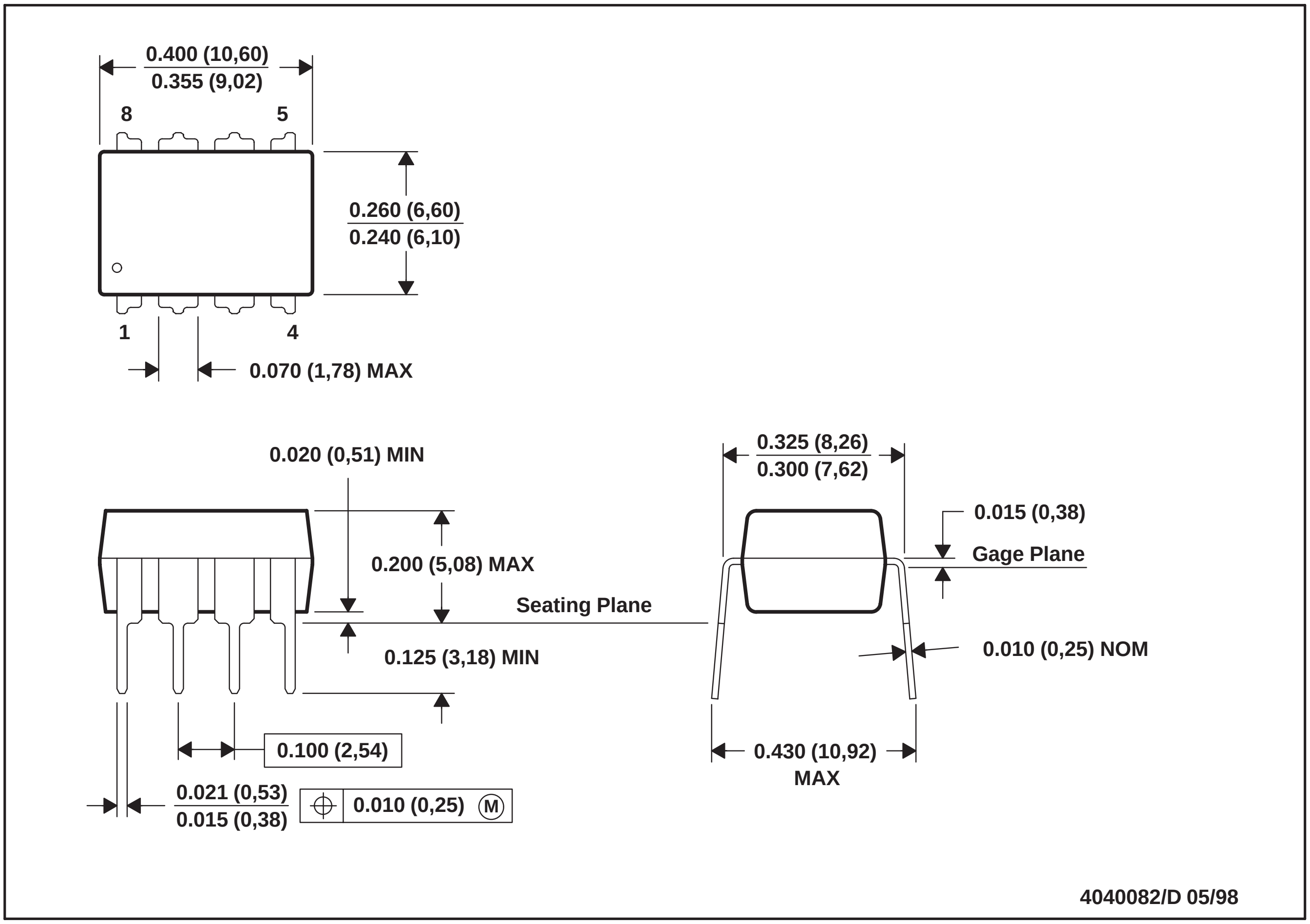

| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.739 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |




4040140 / D 10/96

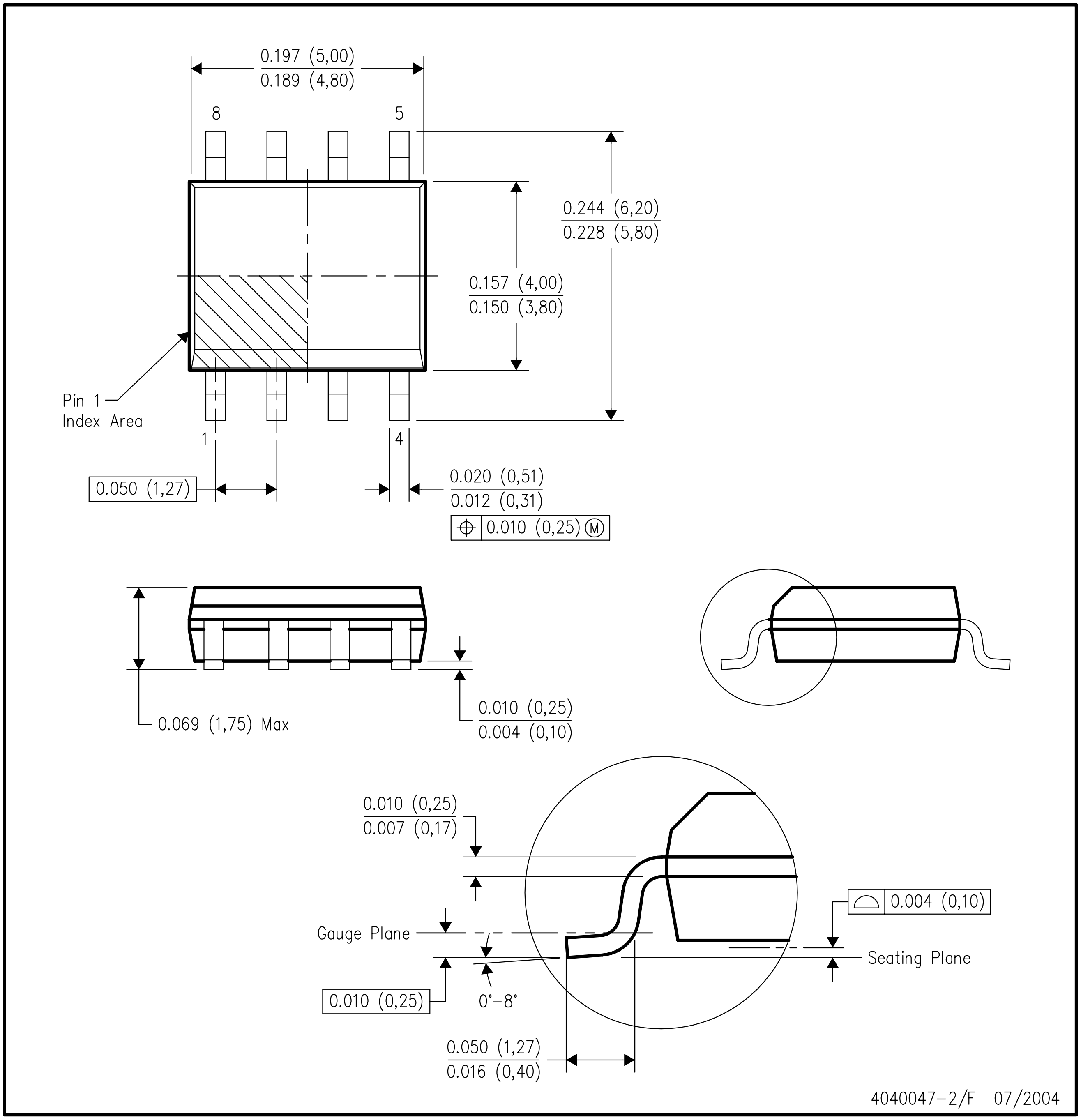
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

**P (R-PDIP-T8)** **PLASTIC DUAL-IN-LINE**

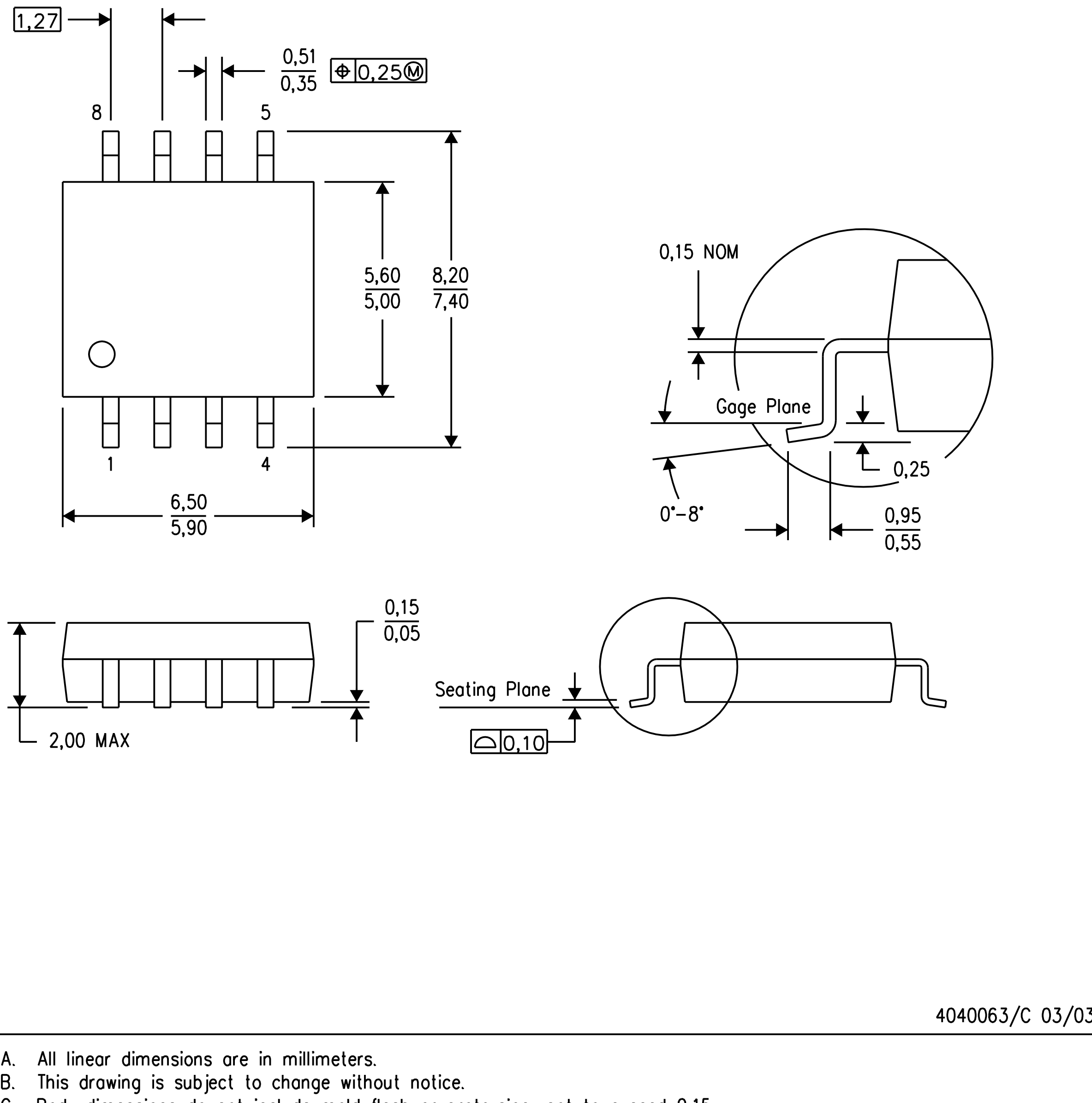



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

# D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



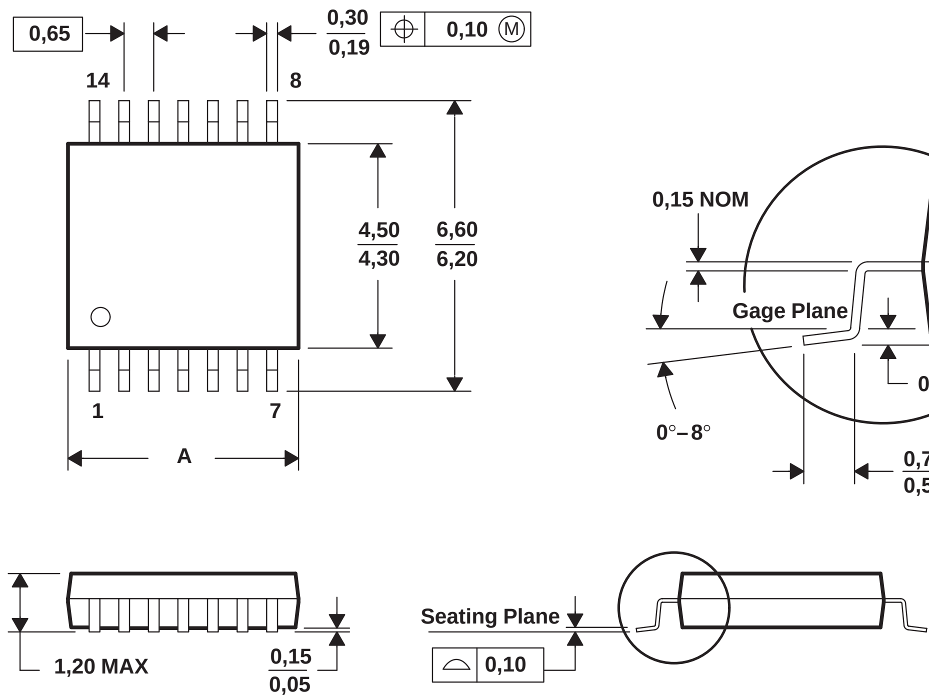

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| PINS ** / DIM | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

| **Products** | | **Applications** | |
|---|---|---|---|
| Amplifiers | amplifier.ti.com | Audio | www.ti.com/audio |
| Data Converters | dataconverter.ti.com | Automotive | www.ti.com/automotive |
| DSP | dsp.ti.com | Broadband | www.ti.com/broadband |
| Interface | interface.ti.com | Digital Control | www.ti.com/digitalcontrol |
| Logic | logic.ti.com | Military | www.ti.com/military |
| Power Mgmt | power.ti.com | Optical Networking | www.ti.com/opticalnetwork |
| Microcontrollers | microcontroller.ti.com | Security | www.ti.com/security |
| | | Telephony | www.ti.com/telephony |
| | | Video & Imaging | www.ti.com/video |
| | | Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265